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Development of Large Diameter High-Purity Semi-Insulating 4H-SiC Wafers for Microwave Devices

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Abstract. The next generation of wireless infrastructure will rely heavily upon wide band gap semiconductors owing to their unique materials properties, including: their large bandgap, high thermal conductivity, and high breakdown field. To facilitate implementation of this next generation, a significant effort is required to make SiC MESFET and GaN HEMT microwave devices more suitable for widespread application. Currently, the interest in high-purity semi-insulating (HPSI) 4H-SiC is critically tied to its influence on microwave devices, whether performance or affordability. To address these issues, we have developed high-purity 3-inch and 100 mm 4H-SiC substrates with low micropipe densities (as low as 1.4 cm^{-2} in 3-inch and <60 cm^{-2} in 100 mm) and uniform semi-insulating properties ($>10^9$ Ωcm) over the full wafer diameter. These wafers possess typical residual shallow level contamination less than $1x10^{16}$ cm^{-3} ($5x10^{15}$ nitrogen and $3x10^{15}$ boron) with best nitrogen values of $3x10^{14}$. In this paper, we will report on the development of our HPSI growth process focusing on the specific areas of the assessment of semi-insulating character and device applicability.

Introduction

Wireless wide-band internet access and video-on-demand is heavily dependent upon the development of a new generation of semiconducting materials which have properties to facilitate highly linear, high power field effect transistors. Due to its unique materials properties[1], silicon carbide has great potential to make significant inroads in the wireless arena. However, semi-insulating (SI) substrates are required to take advantage of these properties for microwave devices. The most common mechanism for the formation of semi-insulating semiconductors is through the use of deep-level dopants which pin the Fermi level to near the middle of the bandgap. After decades of research in SiC, the only viable deep level dopant that has emerged is vanadium acting both as a deep level donor[2,3] and a deep level acceptor[4]. Although vanadium is used to grow the majority of commercially available SI-SiC substrates, reports[5] suggest that vanadium may not be the optimum deep level dopant for SiC. Analogous to the GaAs developments of the early 80's where Cr was deemed an unsuitable deep-level dopant[6] and the intrinsic EL2 defect arose an alternative, we have investigated the use of intrinsic SiC defects to pin the Fermi level deep enough in the bandgap to produce semi-insulating 4H-SiC wafers. We herein report on the current state of the understanding of the HPSI substrates, including our efforts to better understand the source of the semi-insulating character in HPSI.

High purity, large diameter (3-inch & 100 mm) crystals were grown by the PVT method without the intentional introduction of deep level impurities. Substrates were processed from crystals using conventional semiconductor slicing and polishing methodologies.

Discussion – Electrical Characteristics

The development of a semi-insulating substrate requires two key components. First, a deep electronic level is necessary to trap either electrons or holes and to supply a large activation barrier to their subsequent release. Second, shallow levels are required to supply compensation to the deep electronic level so that the Fermi-level can be pinned to the deep electronic level. In high purity silicon carbide, the shallow electronic levels are the well-known impurities: boron (p-type compensation) and nitrogen (n-type compensation). In contrast to shallow levels, the deep electronic levels in HPSI material are not well understood. Figure 1 is a high-resolution, Corema resistivity map of a typical 3-inch diameter HPSI wafer with a resistivity >4e11 Ωcm. A deep electronic level is responsible for the high resistivity nature, but a closer examination of the fundamentals of the semi-insulating material is required to better understand the HPSI process.

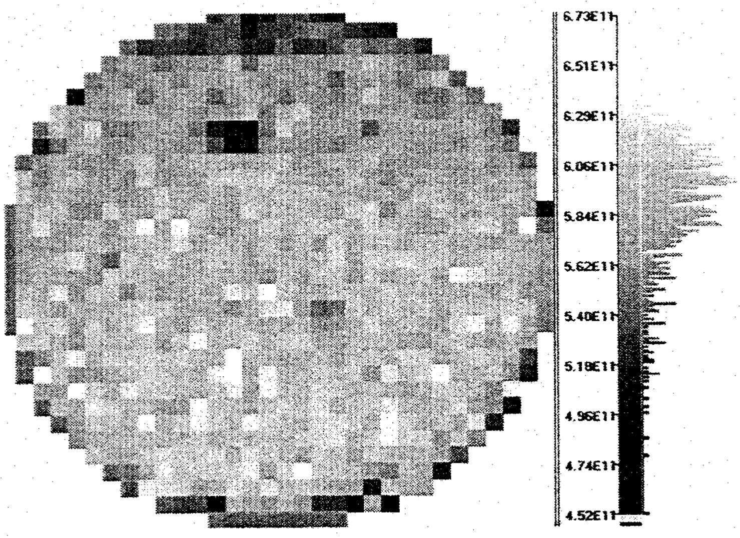

Figure 1 – High resolution resistivity map of a 3-inch diameter 4H-SiC HPSI wafer. The wafer is uniformly semi-insulating with a resistivity $>4\times10^{11}$ Ωcm.

Shallow Electronic Levels. In most semiconductor systems, the term shallow electronic level implies a level residing quite close to either the valence or conduction band edges (typically within 100 meV). In silicon carbide, owing to its much larger bandgap, this definition is typically expanded to include not only nitrogen (E_C - 40 meV) but also boron, even though, in the 4H polytype, boron resides ~ 350 meV above the valence band edge.

Table 1 – SIMS analysis of 4H-SiC HPSI material. The only elements detected are the shallow level impurities nitrogen and boron.

Element	Concentration [cm-3]
B	3.00E+15
N	5.00E+15
Na*, Al*	<5.00E+13
Ti*	1.00E+14
V*, Cr*	5.00E+13
Fe*, P*	2.00E+14
Ni*, F*	5.00E+14
Cu*	3.00E+14
O#	4.00E+16
S*, Cl*	1.40E+15
As*	7.00E+14

* value at SIMS detection limit

value at instrument background limit

Table 1 is a listing of impurities in typical HPSI wafers that have been analyzed using a calibrated SIMS technique. Of the principal shallow level impurities, only boron and nitrogen are present in appreciable quantities, typically 5e15 cm^{-3} and 3e15 cm^{-3}, respectively. These concentrations have been reduced by almost two orders of magnitude during the past three years as the process has been refined. This reduction has significantly expanded our ability to successfully grow HPSI material.

As the level of nitrogen has been reduced, properly measuring its concentration is problematic. The detection limit for nitrogen in a SIMS chamber well conditioned for this specific purpose is around 2e15 cm^{-3}. As the typical nitrogen concentration is reduced in SiC crystals, the nitrogen in our R&D best wafers has fallen below the detection limit of the SIMS, and a new method of nitrogen quantification is required. To solve this problem a technique borrowed from SiC epitaxy has been employed, low temperature photoluminescence (LTPL) detection.[7] In this technique, the ratio of the Q_0 to the I_{75} peak has been shown empirically to be proportional to the nitrogen concentration in the single crystal SiC. Figure 2 is a LTPL plot of a PVT-grown SiC sample with a nitrogen concentration of 3e14 cm^{-3}.[8] This value is the lowest ever reported for nitrogen in bulk-grown SiC.

Deep Electronic Levels. In addition to listing all of the common shallow impurities in SiC, Table 1 also lists all common metallic impurities in SiC. Since each of these is below the detection limit of the SIMS technique, metallic impurities, such as vanadium, cannot be responsible for the deep electronic levels. As a result, intrinsic point defects must be involved in the creation of high resistivity material. Several techniques have been employed to isolate the specific defects responsible for the electronic nature of HPSI material, including: temperature dependent resistivity, optical admittance spectroscopy (OAS), and electron paramagnetic resonance (EPR).

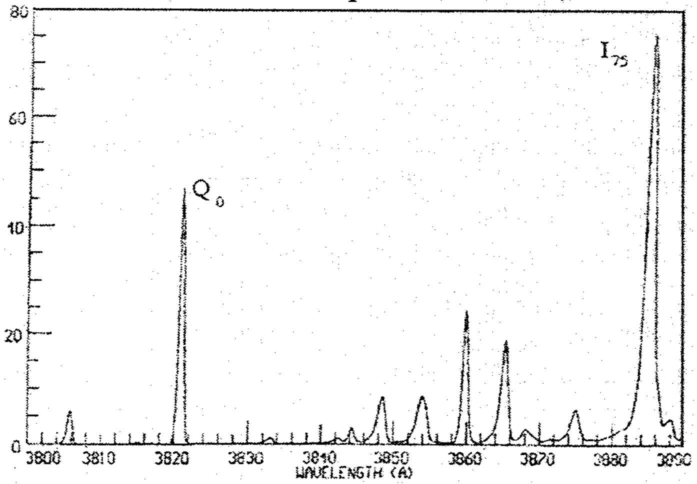

Figure 2 – Near band-edge LTPL of a 4H-SiC HPSI wafer with a calculated nitrogen concentration of 3e14 cm^{-3} determined by taking the ratio of Q_0 to I_{75}.

Temperature dependent resistivity and OAS have been employed in conjunction to identify the depth of the electronic levels present in HPSI material. Figure 3 is a plot of three representative HPSI samples with activation energies of (a) 1.2, (b) 1.35, and (c) 1.5 eV. In addition to these, activation energies in HPSI samples have been measured with values of 0.9, 1.1, and 1.6 eV. The proximity of these energies to one another raises a question as to their uniqueness. This is addressed on two points. First, hundreds of samples were measured, and these energies were determined based upon a statistically significant number of samples with a sufficient degree of separation. Second, analysis of OAS data (Fig. 4) reveals five separate activation energies in a single sample with a very good degree of similarity between the resistivity data and the OAS spectrum. Earlier HPSI substrates, activation energies determined by temperature dependent resistivity typically varied significantly across a wafer. However, as the process has been refined, wafers have been found which possess very good uniformity of activation energies across the entire wafer area (Fig 5).

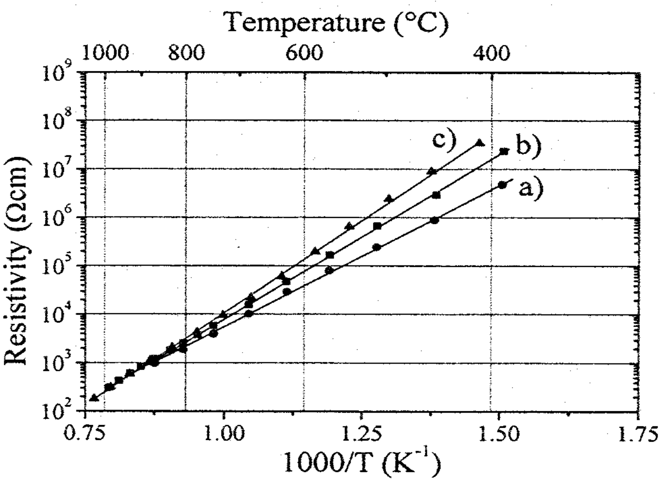

Figure 3 – Resistivity versus temperature for three 4H-SiC HPSI samples whose activation energies are: a) 1.10 eV, b) 1.35 eV, and c) 1.48 eV.

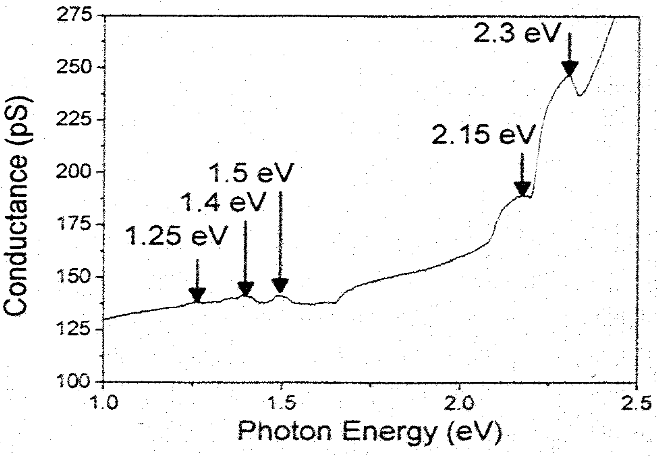

Figure 4 – Admittance versus photon energy plot that reveals the presence of 5 distinct energy levels. Courtesy of W.C. Mitchell and S. Smith.

With the discovery of several activation energies in a large number of samples, the scenario whereby multiple defects are responsible for the semi-insulating character of the wafers is possible. To resolve the specific mechanism, the first step is to identify the structure of the various defects responsible for the electronic levels. The number of point defects may not be as numerous as that of the electronic levels, because deep levels may have multiple energy levels in the bandgap, as is the case of vanadium in SiC. Several analytical techniques have been employed in other semiconductor systems for structural identification, including localized vibrational mode (LVM) spectroscopy, optical absorption, and a variety of magnetic resonance techniques.

	1.62	1.51	1.59	
1.58	1.49	1.51	1.34	1.58
1.47	1.50	1.43	1.53	1.58
1.45	1.40	1.46	1.40	1.58
	1.48	1.50	1.55	

Figure 5 – Activation energy map based upon temperature dependant resistivity data showing very good activation energy uniformity across an entire 3-inch wafer.

Because of its wide applicability and range of samples in which it can be employed, LVM spectroscopy would be very useful in identifying the intrinsic point defects in HPSI SiC.[9] The main problem is that the phonon energy gap in SiC is narrow, and only a few defects have been observed in this range. Therefore, LVM spectroscopy has not proven to be useful for the identification of point defects in HPSI.

Under certain circumstances, optical absorption can be very useful for the identification of the character of the defect, provided the fine structure of the absorption spectrum contains sufficient detail. A large number of HPSI samples were subjected to low temperature (12K) optical absorption. Several previously unidentified features were observed, but each respective structure consisted of not more than a single peak. As such, no definitive conclusions can be made regarding the structure of the responsible point defects.

Contrary to the optical techniques, magnetic resonance techniques have been employed successfully to identify several intrinsic point defects in SiC, including the carbon vacancy, the silicon antisite, and the carbon vacancy-carbon antisite pair. Each of these defects was initially identified in irradiated material, and therefore, the first step is to determine whether or not they are present in unirradiated SiC. Figure 6 is an electron paramagnetic resonance (EPR) spectrum of as-grown HPSI material. The carbon vacancy signature is clearly evident in the spectrum and has been observed in a significant number of HPSI samples. Previous photo-EPR data[10] have suggested that the carbon vacancy resides between 0.9 and 1.2 eV above the valance band edge. Based upon the ubiquitous nature of the carbon vacancy, and the identification of a specific activation energy through photo-EPR, this defect is thought to be one component of the semi-insulating character in HPSI material.

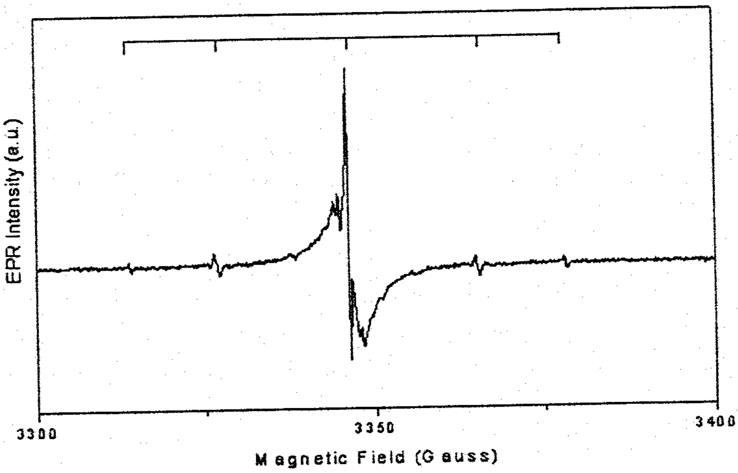

Figure 6 – EPR spectrum of a 4H-SiC HPSI sample whose Fermi level was pinned to the 1.5 eV level and reveals the presence of a carbon vacancy.

In addition to the carbon vacancy, several other intrinsic point defects have been identified in as-grown HPSI material, including the carbon vacancy-carbon antisite pair, the silicon vacancy, and the silicon antisite.[11] Other defects may be present, including ones that may be diamagnetic and therefore not observable by EPR. After identifying several point defects, the next step is to identify the principal point defect or defects responsible for the deep electronic levels from which the semi-insulating character of HPSI is derived. This step involves the quantification of respective deep level concentrations, identification of capture cross-sections, and determination of the defect's electronic structure, each of which is currently underway.

Discussion – Other Characteristics

High electrical resistivity is a critical component in the development of substrates for high power SiC MESFETs. The two other principal considerations are the substrate micropipe density and thermal conductivity. At sufficiently high micropipe densities, a significant impact on the yield of devices is possible owing to the interaction between micropipes and electric fields.[12] Similarly, high thermal conductivity is extremely important to allow for the dissipation of the high levels of waste power generated during device operation.

Micropipe Densities. Micropipes are a unique feature in SiC materials. A major technical goal is to establish the lowest feasible micropipe densities in substrates for devices. Figure 7 is a micropipe map of a high quality 3-inch HPSI substrate. The map was obtained by carefully inspecting the full area of a wafer on a grid of 1.25 mm x 1.25 mm cells for micropipes. As can be seen, a significant fraction of the wafer is free of micropipes (>98% of cells were micropipe free) and the overall micropipe density was very low (1.4 cm^{-2}). Typical micropipe levels are above this R&D best value, and, on a sampled basis, range from 20 to 80 cm^{-2}.

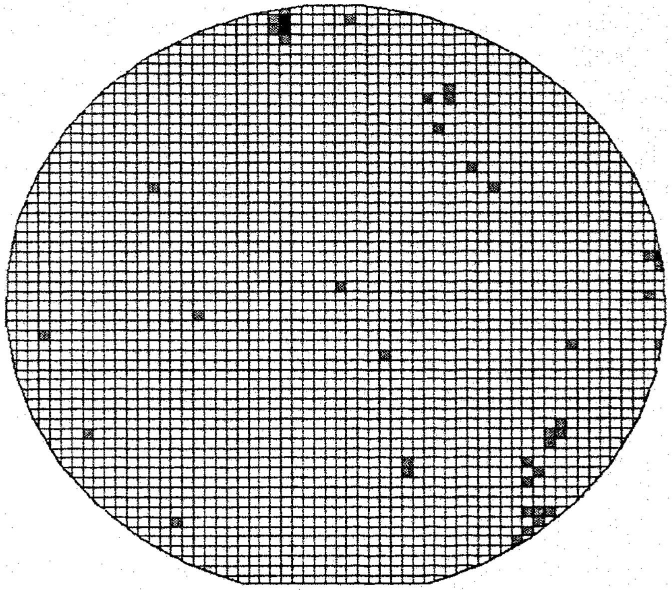

Figure 7 – Micropipe density map of a 3-inch HPSI wafer with a density of 1.4 cm^{-2}. Key for number of micropipes in a cell: white: 0, gray: 1-3, black: >3.

Thermal Conductivity. To more fully understand this extremely important characteristic of our HPSI material, we have employed two types of thermal conductivity measurements (the flash method and scanning thermal microscopy). Previous reports[13] have discussed the flash method measurements on Cree's HPSI material. The thermal conductivity of HPSI (4.9 W/cm·K) approaches the theoretical limit for 4H-SiC based upon the theory developed by Callaway[14], using only U and N processes. Additional measurements using scanning thermal microscopy showed that the thermal conductivity was constant across the wafer. This uniform, extremely high thermal conductivity is essential for the creation of the next generation of electronic devices envisioned for SiC.

SiC MESFET Devices. The main test for any substrate in is its performance as part of a device structure. Devices fabricated on HPSI 4H SiC substrates have resulted in the best combination of power density and efficiency reported to date for SiC MESFETs of 5.2 W/mm and 63% power added efficiency (PAE) at 3.5 GHz, as shown in the load-pull measurements of Fig. 8. Cree recently demonstrated a balanced amplifier using two commercial MESFETs (CRF-22010: 48V class-A operating at 10W and featuring a gain of 12dB at 2.2 GHz) on HPSI substrates that provides 22 W across 2.0-2.4 GHz.[15]

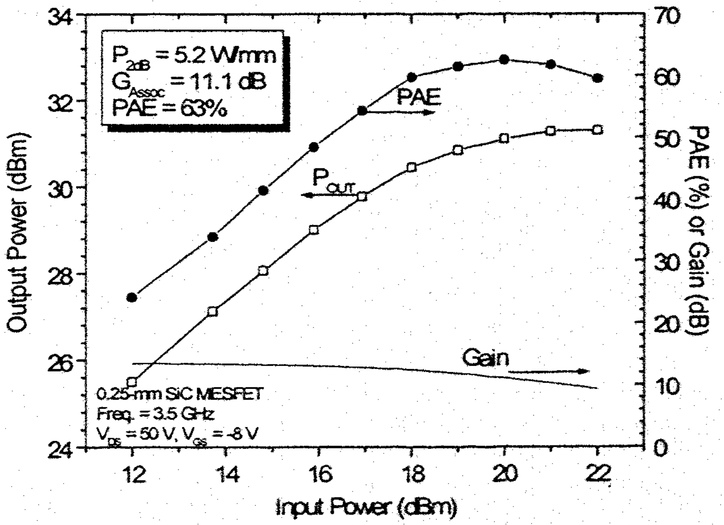

Figure 8 – A 3.5 GHz CW power sweep of a 0.25-mm SiC MESFET on a HPSI 4H SiC substrate tuned in class A operation. V_{DS} = 50 V.

Conclusions

During the past three years a significant effort has been made to create an optimized substrate for SiC MESFET and GaN HEMT device applications. These efforts have culminated in the development of the 4H-SiC HPSI wafer using conventional PVT technology. Along with the creation of the HPSI wafer, efforts have been underway to understand the physics underpinning the semi-insulating character of these high purity substrates including the identification of several electronic levels, intrinsic point defects, and the principal shallow level impurities. However, more work is required to develop a level of understanding akin to that of SI-GaAs. Even without this underlying knowledge, HPSI wafers have been shown to possess the requisite properties to allow for the development of commercially available high quality SiC MESFETs.

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